

Lecture No 5

Addressing & Memory

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Three levels of addressing:

1. *The Process or User Program Level:* At this level the main concern is with efficient representation of user program statements.
2. *The Operating System Level:* Multiple processes sharing a fixed address space. Issues include relocation and protection
3. *The Hardware Manager or Memory Level:* This is the set of physical locations used to interpret level 1 and level 2 addresses. The issues here are access time and prediction of localities which are about to be used.

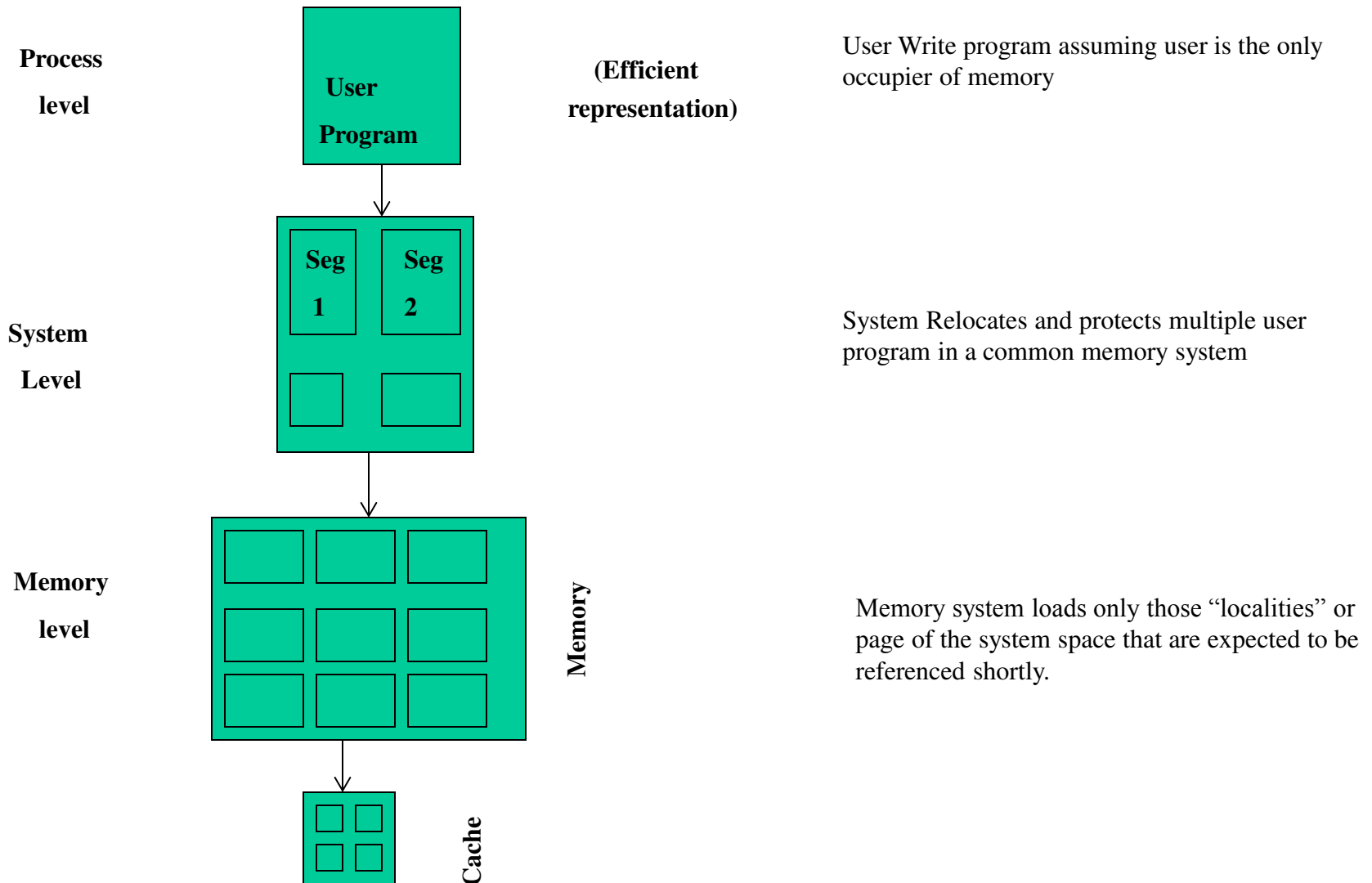
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Addressing & Memory (Contd..)

Three levels of addressing



Addressing & Memory (Contd..)

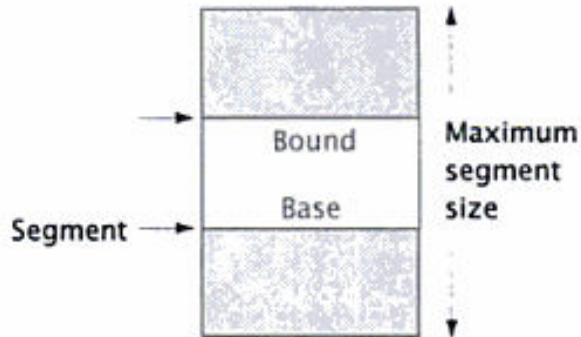
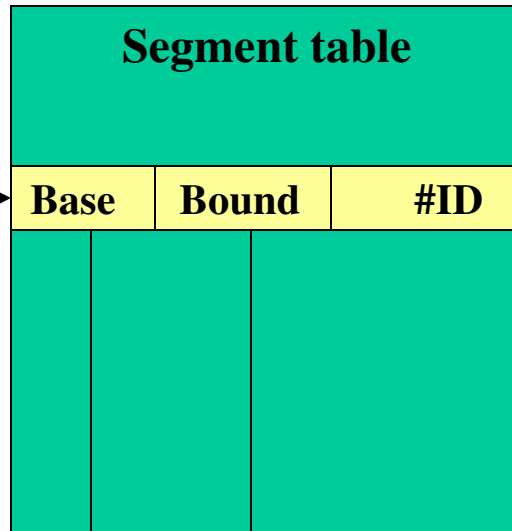
Process or User Program level Addressing

- **Facility to address large number of objects.**
- **The basic address resolution is to the byte.**
- **Most processors adopt an Offset + Base (offset [R_B]) address format.**
- **The contents of base register R_b define the starting point of a region of user memory.**
- **Within this region items are addressed by the offset.**

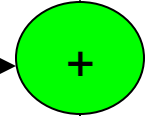
Addressing & Memory (Contd..)

User Process Address

(32 Bits)



Segmented Address



System Address

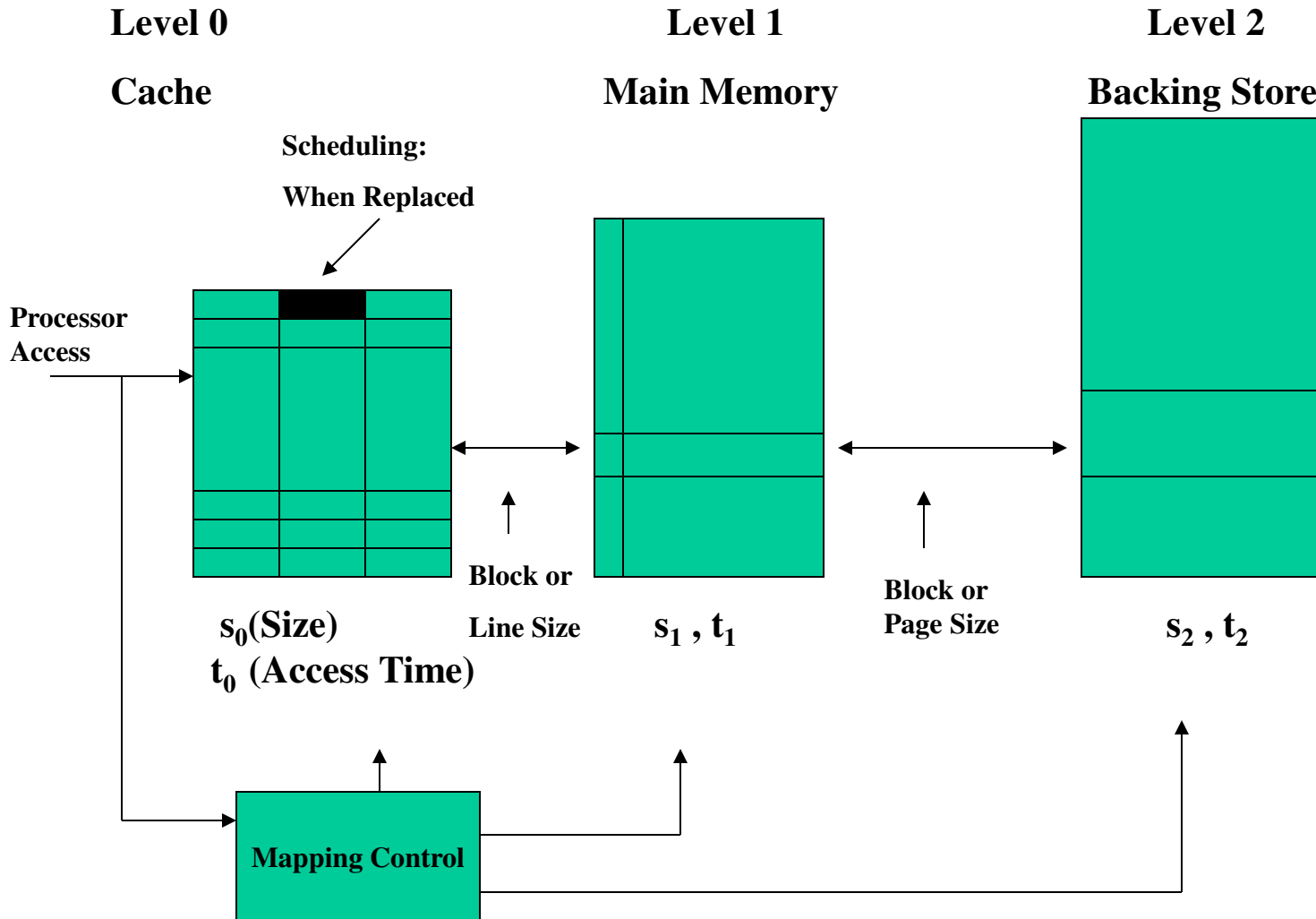
Addressing & Memory (Contd..)

Memory Level

- This level deals with Physical arrangement of memory regions. Based on three parameters
 - ➡ Memory latency,
 - ➡ Memory bandwidth,
 - ➡ Memory size
- Faster levels have greater *cost per bit of storage* so they are generally smaller in size.
- *Cost per bit of storage* goes on decreasing and *access times* goes on increasing as Size of storage grows.
- Typically there are three levels in physical memory hierarchy.
 - ➡ Cache Memory,
 - ➡ Main Memory
 - ➡ Disk and backup storage.

Addressing & Memory (Contd..)

Memory Space



Addressing & Memory (Contd..)

Paging Process :

